LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the pending claims.

1. (Currently Amended) A method for controlling analysis ~~by an analysis tool~~ of multiple instantiations of a circuit in a hierarchical circuit design, the method comprising:

providing a user-selected analysis option to a reliability verification tool ~~the analysis tool~~;

analyzing a first instantiation of the circuit as specified by the analysis option, the first instantiation being selected responsive to the user-selected analysis option provided via a user configuration file supplied in association with the reliability verification tool, wherein the reliability verification tool is operable to analyze electromigration effects with respect to the first instantiation of the circuit; and

responsive to the first instantiation of the circuit passing the analysis, terminating analysis of the circuit.

2. (Original) The method of claim 1 further comprising providing results of the analysis.

3. (Original) The method of claim 1 further comprising, responsive to the first instantiation of the circuit failing the analysis, terminating analysis of the circuit.

4. (Original) The method of claim 3 further comprising providing results of the analysis.

5. (Original) The method of claim 1 further comprising, responsive to the first instantiation of the circuit failing the analysis, analyzing all remaining instantiations of the circuit.

6. (Original) The method of claim 5 further comprising providing results of the analysis.

7. (Original) The method of claim 1 wherein the first instantiation of the circuit comprises a composite worst case instantiation of the circuit, the method further comprising determining a composite worst case instantiation of the circuit.

8. (Original) The method of claim 7 wherein the determining the composite worst case instantiation of the circuit comprises for each net in the circuit:

selecting one of the instantiations having a highest activity factor for the net and assigning the highest activity factor to the net of the composite worst case instantiation;

selecting a logic configuration set that provides a maximum possible switching states for the circuit and assigning the logic configuration to the composite worst case instantiation; and

selecting a maximum of any scale factors that increase loading on signals in the circuit and assigning the selected scale factors to the composite worst case instantiation.

9. (Original) The method of claim 7 further comprising, for each driver in the circuit, selecting an input and output slope combination for the driver that maximizes a crossover current for a signal driven by the driver and assigning the selected input and output slope combination to the driver in the composite worst case instantiation.

10. (Original) The method of claim 7 further comprising selecting a maximum drive fight scale factor and assigning the maximum drive fight scale factor to the composite worst case instantiation.

11. (Currently Amended) The method of claim 1 wherein the first instantiation of the circuit comprises a worst-case instantiation of the circuit ~~the one of the instantiations of the circuit most likely to fail analysis~~.

Claim 12. (Canceled)

13. (Currently Amended) [[An]] A system for analyzing multiple instantiations of a circuit in a hierarchical circuit design, the system comprising:

~~means for receiving a user-selected analysis option;~~

means for analyzing a first instantiation of the circuit ~~as specified by the analysis option~~, the first instantiation being selected responsive to a user-selected analysis option provided via a user configuration file supplied in association with a reliability verification tool, wherein the reliability verification tool is operable to analyze electromigration effects with respect to the first instantiation of the circuit; [[and]]

means responsive to the first instantiation of the circuit passing the analysis for terminating analysis of the circuit; and

means for providing results of the analysis.

14. (Original) The system of claim 13 further comprising, means responsive to the first instantiation of the circuit failing the analysis for terminating analysis of the circuit.

15. (Original) The system of claim 13 further comprising, means responsive to the first instantiation of the circuit failing the analysis for analyzing all remaining instantiations of the circuit.

16. (Original) The system of claim 13 wherein the first instantiation of the circuit comprises a composite worst case instantiation of the circuit, the system further comprising means for determining a composite worst case instantiation of the circuit.

17. (Original) The system of claim 16 wherein the means for determining the composite worst case instantiation of the circuit comprises, for each net in the circuit:

means for selecting one of the instantiations having a highest activity factor for the net;

means for selecting a logic configuration set that provides a maximum possible switching states for the circuit;

means for selecting a maximum of any scale factors that increase loading on signals in the circuit;

means for assigning the highest activity factor to the net of the composite worst case instantiation; and

means for assigning the logic configuration to the composite worst case instantiation and the selected scale factors to the composite worst case instantiation.

18. (Original) The system of claim 16 further comprising, for each driver in the circuit:

means for selecting input and output slope combination for the driver that maximize a crossover current for a signal driven by the driver; and

means for assigning the selected input and output slope combination to the driver in the composite worst case instantiation.

19. (Original) The system of claim 16 further comprising:

means for selecting a maximum drive fight scale factor; and

means for assigning the maximum drive fight scale factor to the composite worst case instantiation.

20. (Currently Amended) The system of claim 13 wherein the first instantiation of the circuit comprises a worst-case instantiation of the circuit ~~the one of the instantiations of the circuit most likely to fail analysis~~.

Claim 21. (Canceled)

22. (Currently Amended) A computer-readable medium operable with a computer for controlling analysis of multiple instantiations of a VLSI circuit in a hierarchical circuit design, the medium having stored thereon:

~~computer-executable instructions for receiving a user-selected analysis option;~~

computer-executable instructions for analyzing a first instantiation of the circuit ~~as specified by the analysis option,~~ the first instantiation being selected responsive to a user-selected analysis option provided via a user configuration file supplied in association with a reliability verification tool, wherein the reliability verification tool is operable to analyze electromigration effects with respect to the first instantiation of the circuit; [[and]]

computer-executable instructions responsive to the first instantiation of the circuit passing the analysis for terminating analysis of the circuit; and

computer-executable instructions for generating results of the analysis.

23. (Original) The medium of claim 22 further having stored thereon computer-executable instructions responsive to the first instantiation of the circuit failing the analysis for terminating analysis of the circuit.

24. (Original) The medium of claim 22 further having stored thereon computer-executable instructions responsive to the first instantiation of the circuit failing the analysis for analyzing all remaining instantiations of the circuit.

25. (Original) The medium of claim 22 wherein the first instantiation of the circuit comprises a composite worst case instantiation of the circuit, the medium further having stored thereon computer-executable instructions for determining a composite worst case instantiation of the circuit.

26. (Original) The medium of claim 25 wherein the computer-executable instructions for determining the composite worst case instantiation of the circuit comprise:

computer-executable instructions for selecting one of the instantiations having a highest activity factor for each the net of the circuit and assigning the highest activity factor to the net of the composite worst case instantiation;

computer-executable instructions for selecting a logic configuration set that provides a maximum possible switching states for the circuit and assigning the logic configuration to the composite worst case instantiation; and

computer-executable instructions for selecting a maximum of any scale factors that increase loading on signals in the circuit and assigning the selected scale factors to the composite worst case instantiation.

27. (Original) The medium of claim 25 further comprising, for each driver in the circuit:

computer-executable instructions for selecting an input and output slope combination for the driver that maximizes a crossover current for a signal driven by the driver and assigning the selected input and output slope combination to the driver in the composite worst case instantiation.

28. (Original) The medium of claim 25 further comprising:

computer-executable instructions for selecting a maximum drive fight scale factor and assigning the maximum drive fight scale factor to the composite worst case instantiation.

29. (Currently Amended) The medium of claim 22 wherein the first instantiation of the circuit comprises a worst-case instantiation of the circuit ~~the one of the instantiations of the circuit most likely to fail analysis~~.

Claim 30. (Canceled)